TRAFFIC LIGHT CONTROLLER

Milwaukee Area Technical College

Preliminary

TITLE: Traffic Light Controller PROJECT: Lab 30		Lab Partner(s):	1200 South 71st Street West Allis, WI 53214, USA (414) xxx-xxxx FAX: (414) xxx-xxxx Email: xxx@matc.edu		
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1 BACKGROUND INFORMATION

In this lab, a traffic light controller will be programmed using VHDL. The sequence and patterns of lights are controlled by a sequence of states, and the order of the states can be altered by the state of the inputs. This allows a walk switch to alter the normal pattern of lights to include the walk signal in the next green cycle.

2 REVISION CONTROL

DATE	CHANGES	REVISION
11/09/2008	INITIAL DRAFT	0.0

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3 DESIGN FILE

3.1 Mod 5 Counter VHDL

```
--timer5.vhd
-- 3 bit mod 5 counter
--Jody Decker

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.STD_LOGIC_UNSIGNED.ALL;

ENTITY timer5 IS
	PORT(
		CLOCK, RESET	: IN STD_LOGIC;
		Q		: BUFFER STD_LOGIC_VECTOR (2 DOWNTO 0));
	END timer5;

ARCHITECTURE a OF timer5 IS
BEGIN
	PROCESS (CLOCK, RESET)
	BEGIN
	IF (RESET = '1') THEN Q <= "000";
	ELSIF (CLOCK'EVENT AND CLOCK = '1') THEN
		IF Q >= "100" THEN
		Q <= "000";
		ELSE Q <= Q + 1;
		END IF;
	END IF;
END PROCESS;
END a;
```


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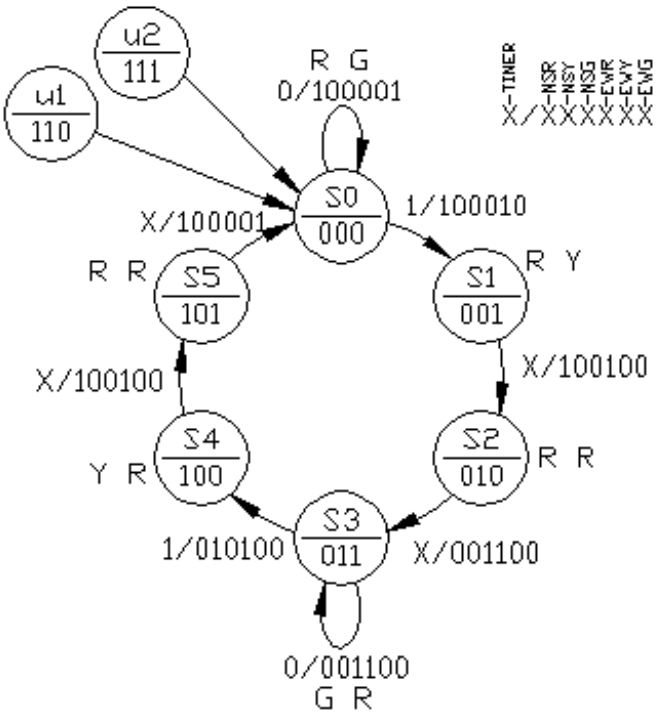

Fig. 1
State Diagram for Traffic Light Controller - Part 1

3.2 Traffic Light Controller VHDL - Part 1

```
--traffic.vhd
--traffic light controller state machine
--Jody Decker

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY traffic IS
        PORT(
                CLK, TIMER, RESET : IN STD_LOGIC;
                Q                 : OUT STD_LOGIC_VECTOR (5 DOWNTO 0));
        END traffic;
```


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```
ARCHITECTURE a OF traffic IS
        TYPE SEQUENCE IS (S0, S1, S2, S3, S4, S5);
        SIGNAL light_state : SEQUENCE;
BEGIN
        PROCESS (CLK, RESET)
        BEGIN
                IF (RESET = '1') THEN
                light_state <= S0;
                Q               <= "100001";
                ELSIF (CLK'EVENT AND CLK = '1') THEN
                        CASE light_state IS
                        WHEN S0     =>
                                IF TIMER = '0' THEN
                                        light_state     <= S0;
                                        Q               <= "100001"; --red grn WAITING
FOR CLK
                                ELSIF TIMER = '1' THEN
                                        light_state     <= S1;
                                        Q               <= "100010"; --red yel
                                END IF;
                        WHEN S1 =>
                                light_state     <= S2;
                                Q               <= "100100"; --red red
                        WHEN S2 =>
                                light_state     <= S3;
                                Q               <= "001100"; --grn red
                        WHEN S3 =>
                                IF TIMER = '0' THEN
                                light_state     <= S3;
                                Q               <= "001100"; --grn red WAITING FOR
CLK
```


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```
            ELSIF TIMER = '1' THEN
                light_state     <= S4;
                Q               <= "010100"; --yel red
                END IF;
            WHEN S4 =>
                light_state     <= S5;
                Q               <= "100100"; --red red
            WHEN S5 =>
                light_state     <= S0;
                Q               <= "100001"; --red grn
            WHEN OTHERS =>
                light_state     <= S0;
                Q               <= "100001"; --red grn
            END CASE;
        END IF;
    END PROCESS;
END a;
```


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3.3 Traffic Controller with Timer VHDL – (Part 1)

```
--traf_and_timer.vhd
--combines traffic controller part1 with timer
--JODY DECKER

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY traf_and_timer IS
        PORT (
                CLK_TLH, RES_TLH                : IN     STD_LOGIC;
                NSR, NSY, NSG, EWR, EWY, EWG : OUT      STD_LOGIC);

END traf_and_timer;

ARCHITECTURE a OF traf_and_timer IS
        COMPONENT timer5
                PORT(
                CLOCK, RESET      : IN STD_LOGIC;
                Q                 : BUFFER STD_LOGIC_VECTOR (2 DOWNTO 0));
                END COMPONENT;

        COMPONENT traffic
                PORT(
                CLK, TIMER, RESET        : IN STD_LOGIC;
                Q                 : OUT STD_LOGIC_VECTOR (5 DOWNTO 0));
                END COMPONENT;

        SIGNAL tim_to_traf : STD_LOGIC;
```


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```
BEGIN
        tmr_1: timer5
        PORT MAP (CLOCK         => CLK_TLH,
                  RESET         => RES_TLH,
                  Q(2)    => tim_to_traf);

        TRAF_1: traffic
        PORT MAP (CLK     => CLK_TLH,
                  RESET         => RES_TLH,
                  TIMER         => tim_to_traf,
                  Q(5)    => NSR,
                  Q(4)    => NSY,
                  Q(3)    => NSG,
                  Q(2)    => EWR,
                  Q(1)    => EWY,
                  Q(0)    => EWG);

        END a;
```


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3.4 Traffic Controller with Timer - Board Test VHDL – (Part 1)

```
--traffic_test_1.vhd
--combines traffic controller part1 with timer and clkdiv2
--JODY DECKER

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY traffic_test_1 IS
        PORT (
                CLK_IN, RES_TLH          : IN     STD_LOGIC;
                NSR, NSY, NSG, EWR, EWY, EWG : OUT      STD_LOGIC);

END traffic_test_1;

ARCHITECTURE a OF traffic_test_1 IS
        COMPONENT timer5
                PORT(
                CLOCK, RESET     : IN STD_LOGIC;
                Q                : BUFFER STD_LOGIC_VECTOR (2 DOWNTO 0));
                END COMPONENT;

        COMPONENT traffic
                PORT(
                CLK, TIMER, RESET        : IN STD_LOGIC;
                Q                : OUT STD_LOGIC_VECTOR (5 DOWNTO 0));
                END COMPONENT;

        COMPONENT clkdiv2
```


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```
        PORT(
        clk             : IN    STD_LOGIC;
        clk_out         : OUT STD_LOGIC);
        END COMPONENT;

SIGNAL tim_to_traf : STD_LOGIC;
SIGNAL clk_sig : STD_LOGIC;

BEGIN
        tmr_1: timer5
        PORT MAP (CLOCK         => clk_sig,
                  RESET         => RES_TLH,
                  Q(2)    => tim_to_traf);

        TRAF_1: traffic
        PORT MAP (CLK     => clk_sig,
                  RESET         => RES_TLH,
                  TIMER         => tim_to_traf,
                  Q(5)    => NSR,
                  Q(4)    => NSY,
                  Q(3)    => NSG,
                  Q(2)    => EWR,
                  Q(1)    => EWY,
                  Q(0)    => EWG);

        CDV: clkdiv2
        PORT MAP (clk       => CLK_IN,
                clk_out                 => clk_sig);

        END a;
```


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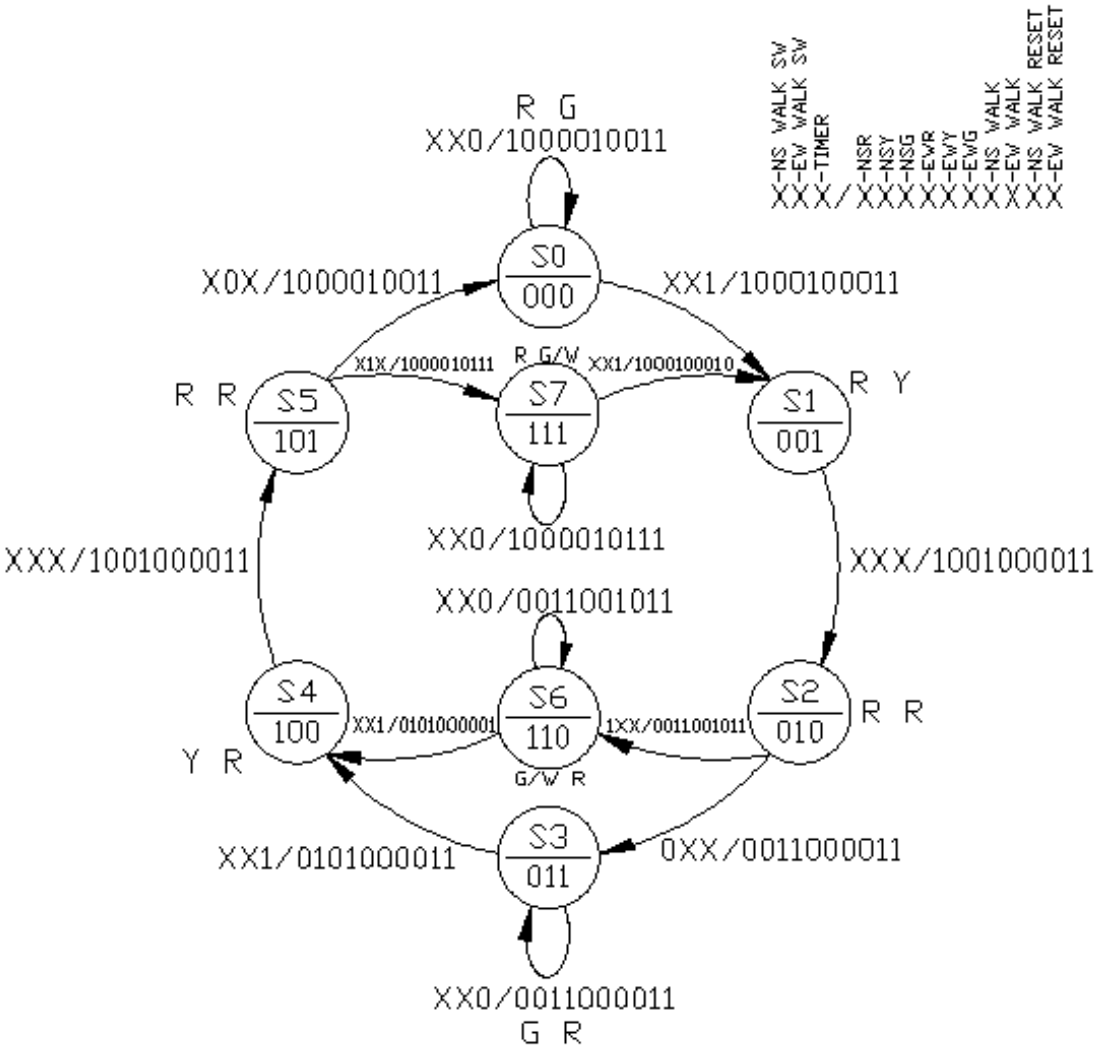

Fig. 2

State Diagram for Traffic Light Controller with Walk Signal – (Part 2)

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3.5 Traffic Light Controller with Walk Signal VHDL – (Part 2)

```
--trafcon_with_walk.vhd
--traffic light controller with in/out& reset for walk signals
--Jody Decker

LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY trafcon_with_walk IS
        PORT(
        CLK, TIMER, RESET, NS_SW, EW_SW : IN STD_LOGIC;
        Q                       : OUT STD_LOGIC_VECTOR (9 DOWNTO 0));
        END trafcon_with_walk;

ARCHITECTURE a OF trafcon_with_walk IS
        TYPE SEQUENCE IS (S0, S1, S2, S3, S4, S5, S6, S7);
        SIGNAL light_state : SEQUENCE;
BEGIN
        PROCESS (CLK, RESET)
        BEGIN
                IF (RESET = '1') THEN
                light_state <= S0;
                Q               <= "1000010011";
                ELSIF (CLK'EVENT AND CLK = '1') THEN
                CASE light_state IS
                WHEN S0     =>
                        IF TIMER = '0' THEN
                                light_state     <= S0;
                Q               <= "1000010011"; --red grn WAITING FOR CLK
```


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```
        ELSIF TIMER = '1' THEN
                light_state     <= S1;
                Q               <= "1000100011"; --red yel
        END IF;
WHEN S1 =>
        light_state     <= S2;
        Q               <= "1001000011"; --red red
WHEN S2 =>
        IF NS_SW = '1' THEN
        light_state     <= S6;
        Q               <= "0011001011";--(grn/walk) RED
        ELSE
        light_state     <= S3;
        Q               <= "0011000011"; --grn red
        END IF;
WHEN S3 =>
        IF TIMER = '0' THEN
        light_state     <= S3;
        Q               <= "0011000011"; --grn red WAITING FOR CLK
        ELSIF TIMER = '1' THEN
        light_state     <= S4;
        Q               <= "0101000011"; --yel red
        END IF;
WHEN S4 =>
        light_state     <= S5;
        Q               <= "1001000011"; --red red
WHEN S5 =>
        IF EW_SW = '1' THEN
        light_state     <= S7;
Q               <= "1000010111"; --red (grn/walk)
ELSE
```


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```
        light_state     <= S0;
        Q               <= "1000010011"; --red grn
        END IF;
        WHEN S6 =>
        IF TIMER = '0' THEN
        light_state     <= S6;
        Q               <= "0011001011"; --(grn/walk) red WAITING FOR CLK
        ELSIF TIMER = '1' THEN
        light_state     <= S4;
        Q               <= "0101000001"; --yel red, reset ns walk sig
        END IF;
        WHEN S7     =>
        IF TIMER = '0' THEN
        light_state     <= S7;
        Q               <= "1000010111"; --red (grn/walk) WAITING FOR CLK
        ELSIF TIMER = '1' THEN
        light_state     <= S1;
        Q               <= "1000100010"; --red yel, reset ew walk sig
                        END IF;
                    WHEN OTHERS =>
                        light_state     <= S0;
                        Q               <= "1000010011"; --red grn
                    END CASE;
                END IF;
        END PROCESS;
END a;
```

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3.6 Traffic Light Controller with Walk Signal - Board Test VHDL – (Part 2)

```
--trafcon_with_walk_test.vhd
--combines traffic controller part2 with timer, clkdiv2, and DFFs
--JODY DECKER

LIBRARY altera;
USE altera.maxplus2.ALL;
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY trafcon_with_walk_test IS
        PORT (
                CLK_IN, RES_TLH, NS_WALK_SW, EW_WALK_SW     : IN      STD_LOGIC;
                NSR, NSY, NSG, EWR, EWY, EWG, CLK_LED : OUT    STD_LOGIC;
                NS_WLK_LT, EW_WLK_LT : OUT STD_LOGIC;
                unused : OUT STD_LOGIC_VECTOR (8 DOWNTO 0));

END trafcon_with_walk_test;

ARCHITECTURE a OF trafcon_with_walk_test IS
        COMPONENT timer5
                PORT(
                CLOCK, RESET          : IN STD_LOGIC;
                Q                     : BUFFER STD_LOGIC_VECTOR (2 DOWNTO 0));
                END COMPONENT;

        COMPONENT trafcon_with_walk
                PORT(
                CLK, TIMER, RESET, NS_SW, EW_SW : IN STD_LOGIC;
                Q                               : OUT STD_LOGIC_VECTOR (9 DOWNTO 0));
                END COMPONENT;
```


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```
        COMPONENT clkdiv2
                PORT(
                clk             : IN    STD_LOGIC;
                clk_out         : OUT   STD_LOGIC);
                END COMPONENT;

        component dff
port(
   d, clk, clrn, prn :  in  std_logic;
   q              :  out std_logic);
        end component;

        SIGNAL tim_to_traf : STD_LOGIC;
        SIGNAL clk_sig : STD_LOGIC;
        SIGNAL ns_sw_sig : STD_LOGIC;
        SIGNAL ew_sw_sig : STD_LOGIC;
        SIGNAL ns_res_sig : STD_LOGIC;
        SIGNAL ew_res_sig : STD_LOGIC;

        BEGIN
                tmr_1: timer5
                PORT MAP (CLOCK     => clk_sig,
                                RESET => RES_TLH,
                                Q(2)     => tim_to_traf);

                TRAF_1: trafcon_with_walk
                PORT MAP (CLK         => clk_sig,
                                RESET => RES_TLH,
                                TIMER  => tim_to_traf,
                                NS_SW=> ns_sw_sig,
                                EW_SW          => ew_sw_sig,
                                Q(9)     => NSR,
                                Q(8)     => NSY,
                                Q(7)     => NSG,
                                Q(6)     => EWR,
```


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```
                Q(5)    => EWY,
                Q(4)    => EWG,
                Q(3)    => NS_WLK_LT,
                Q(2)    => EW_WLK_LT,
                Q(1)    => ns_res_sig,
                Q(0)    => ew_res_sig);

CDV: clkdiv2
PORT MAP (clk => CLK_IN,
        clk_out         => clk_sig);

ns_dff: dff
PORT MAP (d             => '0',
        clk                     => '0',
        clrn            => ns_res_sig,
        prn                     => NS_WALK_SW,
        q                       => ns_sw_sig);

ew_dff: dff
PORT MAP (d             => '0',
        clk                     => '0',
        clrn            => ew_res_sig,
        prn                     => EW_WALK_SW,
        q                       => ew_sw_sig);

UNUSED          <= "000000000";
CLK_LED         <= clk_sig;
END a;
```


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4 SIMULATION RESULTS

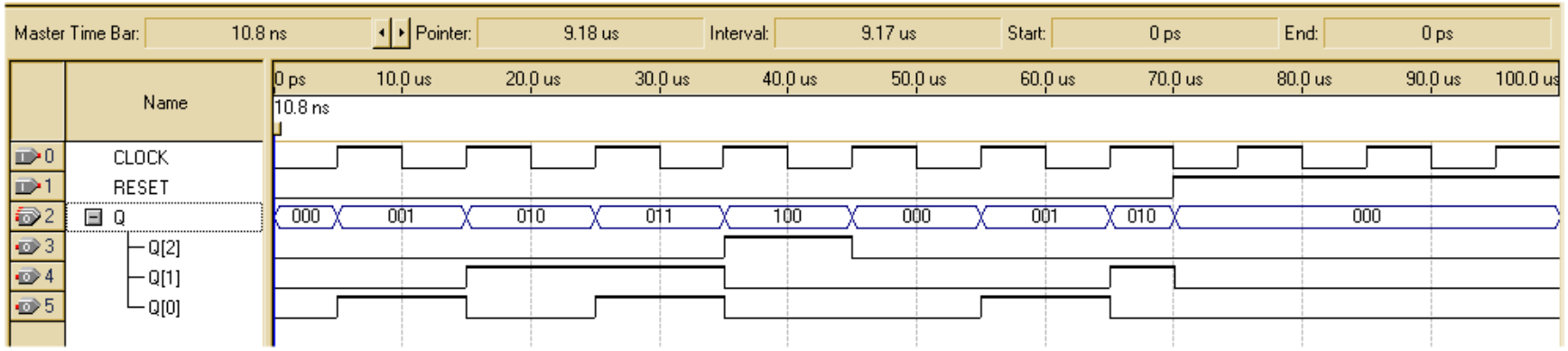

Fig.3 - Simulation Results for Mod 5 Counter

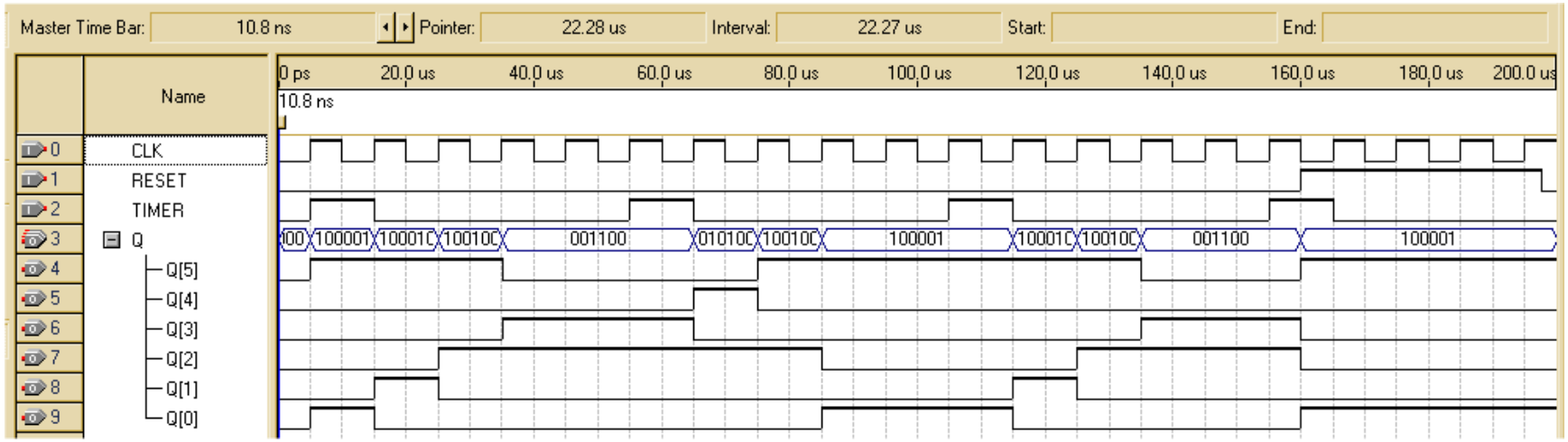

Fig. 4 - Simulation Results for Traffic Light Controller – (Part 1)

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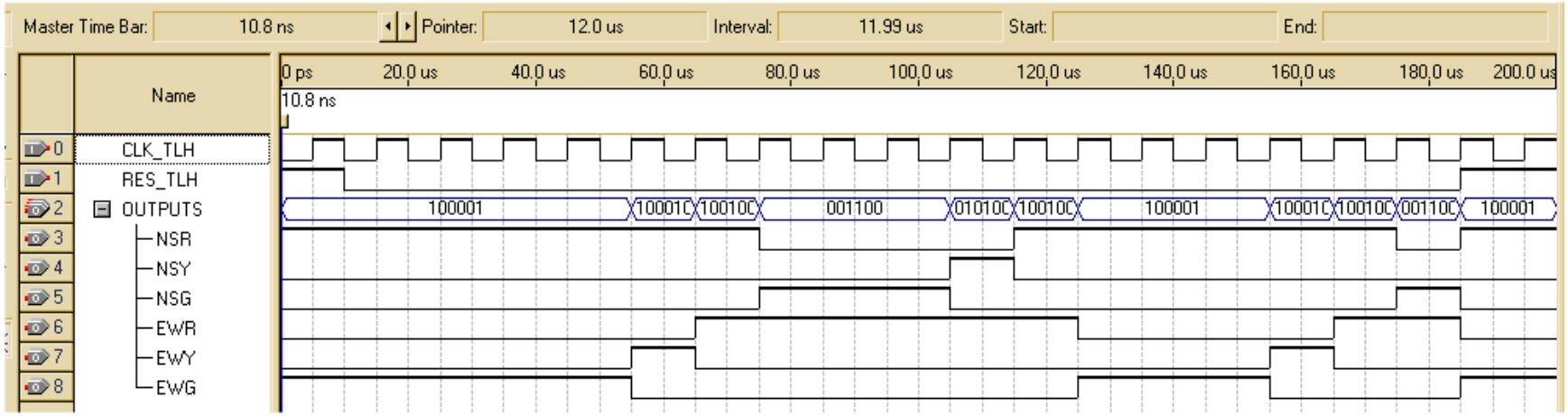

Fig. 5 - Simulation Results for Traffic Light Controller with timer – (Part 1)

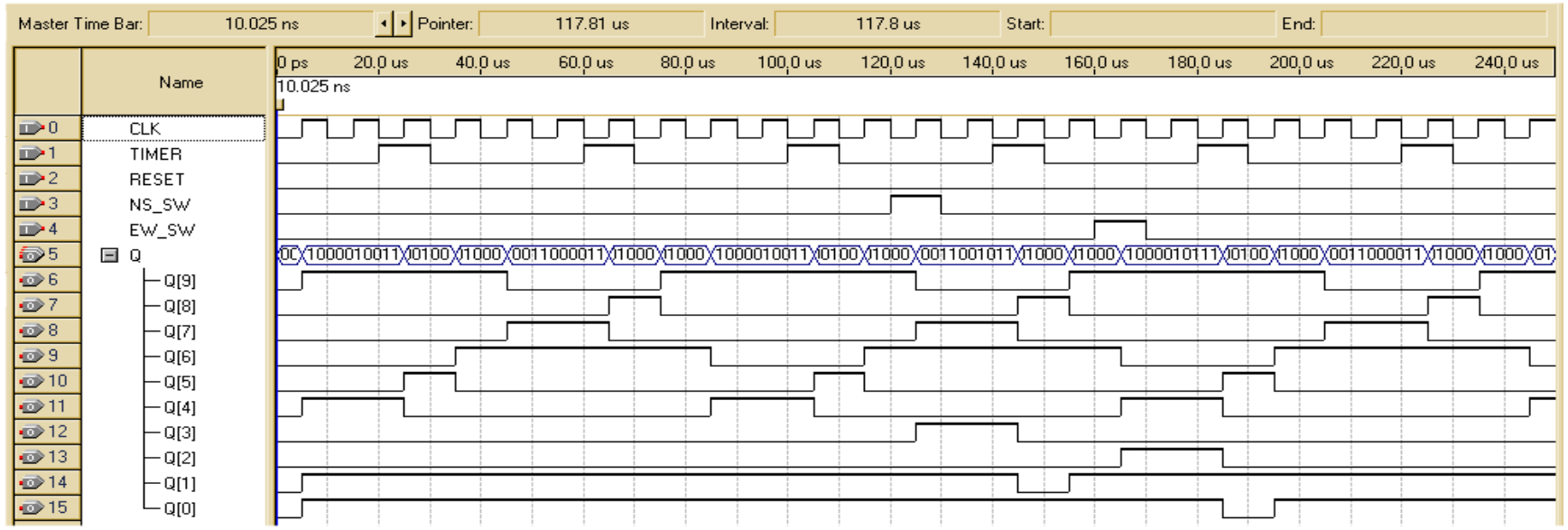

Fig. 6 - Simulation Results for Traffic Controller with Walk Signal (Part-2)

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5 RESULTS

The green light is 3 clock pulses long because the timer pulses once for every five pulses of the clock, and after the timer pulses, there is one clock for yellow and one more for red/red before the next green light turns on. The number of clock pulses that the green light is on will always be 3 less than the clock pulses for red

The frequency of the clock after after the clock divider is

$$f_C = \frac{\text{Frequency of board clock}}{2^{22}} = \frac{4MHz}{2^{22}} = .95Hz$$

$$\text{pulse time} = 1.05\,\text{sec}$$

Board Test results

Traffic Controller Test (Part 1), LEDs cycled through same sequence on the test board as was shown in simulation (Fig. 5)

Traffic controller with walk signal Test (Part 2), LEDs cycled through same sequence on the test board as was shown in simulation (Fig. 6). Walk switches latched on and lit the respective walk LEDs for 1 green cycle when the button was pushed at any time during the cycle, and the latch reset afterwards.

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